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WHAT IS CLAIMED IS:

1 1. A logic circuit, comprising:
2 a first inversion section for inverting a first
3 input signal having one of positive logic and negative
4 logic and outputting the inverted signal;
5 a second inversion section for inverting a second
6 input signal having the other of the positive logic and
7 the negative logic and outputting the inverted signal;
8 and
9 a transmission section for selectively outputting
10 one of the output of said first inversion section and the
11 output of said second inversion section in accordance with
12 a logical value which depends upon an externally
13 controllable selection signal and an inverted signal of
14 the selection signal.

1 2. A logic circuit, comprising:
2 a first inversion section for inverting a first
3 input signal and outputting the inverted signal;
4 a second inversion section for inverting a second
5 input signal and outputting the inverted signal;
6 a first outputting section for selectively
7 outputting one of the output of said first inversion
8 section and the output of said second inversion section
9 in accordance with a logical value which depends upon an
10 externally controllable first selection signal and an
11 inverted signal of the first selection signal; and
12 a second outputting section for selectively

13 ~~outputting one of the output of said first inversion~~
14 ~~section and the output of said second inversion section~~
15 ~~in accordance with a logical value which depends upon an~~
16 ~~externally controllable second selection signal and an~~
17 ~~inverted signal of the second selection signal.~~

1 3. A logic circuit, comprising:
2 a first inversion section for inverting a first
3 input signal and outputting the inverted signal;
4 a second inversion section for inverting a second
5 input signal and outputting the inverted signal; and
6 a transmission section capable of discriminating
7 a magnitude relationship of 1 bit between the first input
8 signal and the second input signal and outputting a result
9 of the discrimination using a plurality of status signals.

1 4. The logic circuit according to claim 3, wherein said
2 transmission section includes a first gate section for
3 indicating whether or not the first input signal is equal
4 to or greater than the second input signal, a second gate
5 section for indicating whether or not the first input
6 signal is greater than the second input signal, a third
7 gate section for indicating whether or not the first input
8 signal is equal to or smaller than the second input signal,
9 and a fourth gate section for indicating whether or not
10 the first input signal is smaller than the second input
11 signal.

1 5. A logic circuit, comprising:
2 a first comparison section for receiving a first
3 input signal of n_1 bits and a second input signal of n_1
4 bits, performing magnitude comparison between a
5 predetermined number of bits of the first input signal
6 and the predetermined number of bits of the second input
7 signal and outputting results of the comparison of the
8 predetermined number of bits as a p_1 th comparison result,
9 a p_2 th comparison result, a p_3 th comparison result and a
10 p_4 th comparison result using a plurality of status signals,
11 n_1 being an integer equal to 2 to the m_1 th power, m_1 being
12 an even number equal to or greater than 2;
13 a second comparison section for performing
14 magnitude comparison between a number of bits equal to
15 twice the predetermined number of bits of the first input
16 signal and a number of bits equal to twice the
17 predetermined number of bits of the second input signal
18 from the p_1 th comparison result and the p_2 th comparison
19 result and outputting a result of the comparison of the
20 predetermined number of bits as a p_5 th comparison result
21 using the plurality of status signals and for performing
22 magnitude comparison between a number of bits equal to
23 twice the predetermined number of bits of the first input
24 signal and a number of bits equal to twice the
25 predetermined number of bits of the second input signal
26 from the p_3 th comparison result and the p_4 th comparison
27 result and outputting a result of the comparison of the
28 predetermined number of bits as a p_6 th comparison result

21 signals;

22 a third arithmetic section for outputting logical
23 AND information of the carries of all of the n_2 bits as
24 a q_7 th carry using the plurality of status signals from
25 at least the q_5 th carry and the q_6 th carry; and

26 a fourth arithmetic section for performing logical
27 exclusive ORing of the output of said half addition
28 arithmetic section and the q_7 th carry and outputting a full
29 addition arithmetic result.

1 7.

A logic circuit, comprising:

2 a first inversion section for inverting a first
3 input signal and outputting the inverted signal;

4 a second inversion section for inverting the
5 inverted signal of the first input signal and outputting
6 a resulting signal;

7 a first outputting section for performing NANDing
8 arithmetic between the output of said first inversion
9 section and a second input signal and outputting a
10 resulting signal; and

11 a second outputting section for performing NANDing
12 arithmetic between the output of said second inversion
13 section and an inverted signal of the second input signal
14 and outputting a resulting signal;

15 said first outputting section and said second
16 outputting section being switched with the second input
17 signal and the inverted signal of the second input signal.

69 a second gate signal of n_3 bits which includes the seventh
70 logical AND inversion result, the eighth logical AND
71 inversion result, the sixth logical AND inversion result
72 and the fourth logical AND result.

1 10. The logic circuit as claimed in claim 3, wherein
2 the plurality of status signals includes a first gate
3 signal for indicating whether or not the first input
4 signal is equal to or greater than the second input signal,
5 a second gate signal for indicating whether or not the
6 first input signal is greater than the second input signal,
7 a third gate signal for indicating whether or not the first
8 input signal is equal to or smaller than the second input
9 signal, and a fourth gate signal for indicating whether
10 or not the first input signal is smaller than the second
11 input signal.

1 11. The logic circuit as claimed in claim 5, wherein
2 the plurality of status signals includes a first gate
3 signal for indicating whether or not the first input
4 signal is equal to or greater than the second input signal,
5 a second gate signal for indicating whether or not the
6 first input signal is greater than the second input signal,
7 a third gate signal for indicating whether or not the first
8 input signal is equal to or smaller than the second input
9 signal, and a fourth gate signal for indicating whether
10 or not the first input signal is smaller than the second

